IN THE CLAIMS

Please amend the claims as follows:

1. (Original) A method of reducing skew between a plurality of signals transmitted with a transmit clock, wherein the plurality of signals includes a first signal and a second signal, the method comprising:

receiving the transmit clock and each of the plurality of signals;

detecting skew between the received transmit clock and each of the received signals;

adding delay to one or more of the plurality of received signals to compensate for the detected skew;

phase comparing each of the plurality of delayed signals to a reference signal to detect changes in the detected skew; and

modifying the delay added to each of the plurality of delayed signals to adapt to changes in the detected skew.

2. (Original) The method of claim 1, wherein phase comparing includes generating a clock early signal and a data early signal for each of the plurality of signals.

3. (Original) The method of claim 2, wherein adding delay includes:

passing each of the plurality of received signals through a separate delay line; and

setting delay as a function of the clock early and data early signals, wherein setting delay includes determining a minimum latency through the delay lines.

4. (Original) The method of claim 3, wherein each delay line includes a plurality of taps and wherein setting delay includes selecting one of the plurality of taps.

5. (Original) The method of claim 3, wherein each delay line includes a plurality of feedback positions and wherein setting delay includes selecting one of the plurality of feedback positions.

6. (Original) The method of claim 1, wherein detecting skew includes:

doubling the received transmit clock to form a doubled clock; and

clocking a phase comparator circuit with the doubled clock.

7. (Original) The method of claim 6, wherein the phase comparator circuit generates a clock early signal and a data early signal for each of the plurality of received signals and wherein adding delay includes:

passing each of the plurality of received signals through a separate delay line; and

setting delay as a function of the clock early and data early signals, wherein setting delay includes determining a minimum latency through the delay lines.

8. (Original) The method of claim 7, wherein each delay line includes a plurality of taps and wherein setting delay includes selecting one of the plurality of taps.

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9. (Original) The method of claim 7, wherein each delay line includes a plurality of feedback positions and wherein setting delay includes selecting one of the plurality of feedback positions.

10. (Original) The method of claim 1, wherein adding delay includes capturing each of the plurality of received signals in an output register.

11. (Original) A circuit for reducing skew between a plurality of signals transmitted with a channel clock, wherein the plurality of signals includes a first and a second signal, the circuit comprising:

a first data capture circuit connected to the first signal, wherein the first data capture circuit includes a first delay line and a first skew detection circuit connected to the first delay line;

a second data capture circuit connected to the second signal, wherein the second data capture circuit includes a second delay line and a second skew detection circuit connected to the second delay line;

a delay line controller connected to the first and second delay lines and the first and second skew detection circuits, wherein the delay line controller receives skew indicator signals representing skew from each of said first and second skew detection circuits and controls delay added by said first and second delay lines; and

a channel clock interface connected to the first and second skew detection circuits, wherein said channel clock interface frequency doubles the channel clock to form a doubled channel clock;

wherein the first and second skew detection circuits detect skew as a function of the doubled channel clock.

12. (Original) The circuit of claim 11, wherein each data capture circuit further includes an output register synchronized to a local clock.

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13. (Original) The circuit of claim 11, wherein the first skew detection circuit includes a phase comparator for comparing phase of the doubled channel clock to the first signal and wherein the second skew detection circuit includes a phase comparator for comparing phase of the doubled channel clock to the second signal.

14. (Original) The circuit of claim 13, wherein the delay line controller includes a digital filter connected to each of the phase comparators.

15. (Original) The circuit of claim 11, wherein the delay line controller includes a digital filter connected to one of said skew indicator signals.

16. (Original) The circuit of claim 11, wherein the channel clock interface includes a duty cycle sensing circuit, wherein the duty cycle sensing circuit is connected to the doubled channel clock and wherein the duty cycle sensing circuit operates with the doubled channel clock to produce an approximately fifty percent duty cycle doubled channel clock.

17. (Original) The circuit of claim 11, wherein each data capture circuit further includes a serial to parallel converter connected to a sampling circuit, wherein the serial to parallel converter and the sampling circuit are clocked with the doubled channel clock.

18. (Original) The circuit of claim 17, wherein the sampling circuit includes a first and second register, wherein the signals are transmitted as bits, wherein the bits are grouped as odd and even groups of bits, and wherein even groups of bits are stored in the first register and odd groups of bits are stored in the second register.

19. (Original) The circuit of claim 17, wherein the serial to parallel converter is a four-bit shift register.

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20. (Original) The circuit of claim 11, wherein each of the first and second delay lines include a fine tune delay line and a coarse tune delay line.

21. (Original) The circuit of claim 11, wherein the skew indicator signals include a clock early signal and a data early signal.

22. (Original) The circuit of claim 11, wherein a core clock signal drives the delay line controller and the output register.

23. (Original) A skew detection circuit, comprising a phase comparator, wherein the phase comparator compares phase of an input signal to a clock signal to generate a clock early signal and a data early signal.

24. (Original) The skew detection circuit of claim 23, wherein the phase comparators include a plurality of flip-flops.

25. (Original) A delay line controller for controlling a plurality of delay lines, wherein each delay line receives an input signal and generates a delayed signal as a function of the input signal, comprising:

a plurality of skew indicator signal inputs, wherein each skew indicator signal input is capable of receiving a skew indicator signal reflecting skew between one of the delayed input signals and a reference signal;

a digital filter connected to each of said plurality of skew indicator signal inputs, wherein each digital filter generates a delay control signal associated with one of the delayed input signals; and

control logic for controlling the plurality of delay lines as a function of the delay control signals.

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26. (Original) The delay line controller of claim 25, wherein the control logic includes a feedback control system which adaptively deskews the input signals.

27. (Original) A communication system, comprising:

a transmitter, wherein the transmitter transmits a plurality of signals in parallel, wherein the plurality of signals includes a first and a second signal; and

a receiver, wherein the receiver includes a deskewing circuit, wherein the deskewing circuit includes:

a first data capture circuit connected to the first signal, wherein the first data capture circuit includes a first delay line and a first skew detection circuit connected to the first delay line;

a second data capture circuit connected to the second signal, wherein the second data capture circuit includes a second delay line and a second skew detection circuit connected to the second delay line;

a delay line controller connected to the first and second delay lines and the first and second skew detection circuits, wherein the delay line controller receives skew indicator signals representing skew from each of said first and second

skew detection circuits and controls delay added by said first and second delay lines; and

a channel clock interface connected to the first and second skew detection circuits, wherein said channel clock interface frequency doubles the channel clock to form a doubled channel clock;

wherein the first and second skew detection circuits detect skew as a function of the doubled channel clock.

28. (Original) The circuit of claim 27, wherein each data capture circuit further includes an output register synchronized to a local clock.

29. (Original) The circuit of claim 27, wherein the first skew detection circuit includes a phase comparator for comparing phase of the doubled channel clock to the first signal and wherein the second skew detection circuit includes a phase comparator for comparing phase of the doubled channel clock to the second signal.

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30. (Original) The circuit of claim 29, wherein the delay line controller includes a digital filter connected to each of the phase comparators.

31. (Original) The circuit of claim 27, wherein the delay line controller includes a digital filter connected to one of said skew indicator signals.

32. (Original) The circuit of claim 27, wherein the channel clock interface includes a duty cycle sensing circuit, wherein the duty cycle sensing circuit is connected to the doubled channel clock and wherein the duty cycle sensing circuit operates with the doubled channel clock to produce an approximately fifty percent duty cycle doubled channel clock.

33. (Original) The circuit of claim 27, wherein each data capture circuit further includes a serial to parallel converter connected to a sampling circuit, wherein the serial to parallel converter and the sampling circuit are clocked with the doubled channel clock.

34. (Original) The circuit of claim 33, wherein the sampling circuit includes a first and second register, wherein the signals are transmitted as bits, wherein the bits are grouped as odd and even groups of bits, and wherein even groups of bits are stored in the first register and odd groups of bits are stored in the second register.

35. (Original) The circuit of claim 33, wherein the serial to parallel converter is a four-bit shift register.

36. (Original) The circuit of claim 27, wherein each of the first and second delay lines include a fine tune delay line and a coarse tune delay line.

37. (Original) The circuit of claim 27, wherein the skew indicator signals include a clock early signal and a data early signal.

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38. (Original) The circuit of claim 27, wherein a core clock signal drives the delay line controller and the output register.

39. (Original) An integrated circuit, comprising:

a transmitter, wherein the transmitter transmits a plurality of signals in parallel, wherein the plurality of signals includes a first and a second signal; and

a receiver, wherein the receiver includes a deskewing circuit, wherein the deskewing circuit includes:

a first data capture circuit connected to the first signal, wherein the first data capture circuit includes a first delay line and a first skew detection circuit connected to the first delay line;

a second data capture circuit connected to the second signal, wherein the second data capture circuit includes a second delay line and a second skew detection circuit connected to the second delay line;

a delay line controller connected to the first and second delay lines and the first and second skew detection circuits, wherein the delay line controller receives

skew indicator signals representing skew from each of said first and second skew detection circuits and controls delay added by said first and second delay lines; and

a channel clock interface connected to the first and second skew detection circuits, wherein said channel clock interface frequency doubles the channel clock to form a doubled channel clock;

wherein the first and second skew detection circuits detect skew as a function of the doubled channel clock.

40. (Original) A method for establishing the phase relationship between a plurality of signals, including a first signal, the method comprising:

initializing signal deskewing circuitry, wherein initializing includes driving the circuitry with a predefined sequence of data edges;

providing a phase comparator;

driving the phase comparator with a clock having 2 edges per data bit and a 50% duty cycle, wherein driving includes sensing the clock and determining an error signal indicating drift from the 50% duty cycle;

determining a phase relationship between the first signal and the clock;

setting delay for the first signal as a function of the phase relationship; and

modifying the delay as a function of changes in the phase relationship.

41. (Original) The method of claim 40, wherein initializing the signal deskewing circuitry further includes establishing delay required in a coarse tune delay line.

42. (Currently Amended) In a system having a channel clock, a plurality of channel signals and delay lines for delaying the channel clock and the plurality of channel signals, a method of adaptively deskewing delays between the plurality of channel signals, comprising:

determining phase relationships between the channel clock and the plurality of channel signals, wherein determining includes generating skew indicator signals for each of the plurality of signals;

filtering each skew indicator signal to reduce jitter;

initializing a data minus clock (DMC) value for each channel signal;

increasing the value of the DMC value corresponding to a particular signal if that signal arrives early with respect to a reference signal;

decreasing the value of the DMC value corresponding to a particular signal if that signal arrives late with respect to the reference signal;

determining a minimum DMC value from the plurality of DMC values;

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if the minimum DMC value is greater than zero, setting delay of the clock delay line to a minimum;

if the minimum DMC value is less than zero, setting delay of the clock delay line to the absolute value of the minimum DMC value;

calculating a channel signal delay for each of the channel signals, wherein calculating a delay includes determining a difference between the minimum DMC value and the DMC value corresponding to each of the plurality of channel signals; and

setting delay of each of the channel signal delay lines to the channel signal delay calculated for each of the channel signals.